Claims

[c1] What is claimed is:

A method of repeatedly exposing a pattern across a wafer, said method comprising:

exposing said pattern at a first location of said wafer, wherein said pattern includes at least one alignment mark; and

repeating said exposing process across said wafer, such that said pattern is repeatedly printed across said wafer,

wherein said process of repeating said exposing process erases said alignment mark from portions of said wafer where said pattern was previously exposed.

[c2] The method in claim 1, wherein each time said exposing process is repeated, the current exposure overlaps a portion of said wafer where said pattern was previously exposed.

[c3] The method in claim 1, wherein said process of repeating said exposing process erases said first alignment mark by re-exposing an area of said wafer where said first alignment mark was previously exposed.

[c4] The method in claim 1, wherein each repetition of said exposing process across said wafer erases a previous alignment mark.

[c5] The method in claim 1, wherein, after said exposing process is repeated across said wafer, alignment marks remain only on

the edge of said wafer.

[c6] The method in claim 1, wherein said exposing process and said process of repeating said exposing process utilize the same mask to expose said pattern.

[c7] The method in claim 6, wherein said mask includes a transparent region at a location where an image produced by a subsequent exposing process overlaps a previously exposed alignment mark.

[c8] A method of exposing chips on a wafer, said method comprising:
a first exposing process of exposing at least one first integrated circuit chip and at least one first alignment mark on a wafer; and
a second exposing process of exposing at least one second integrated circuit chip, adjacent said first integrated circuit chip, and at least one second alignment mark on said wafer, wherein said second exposing process erases said first alignment mark.

[c9] The method in claim 8, wherein said second exposing process overlaps area of said wafer exposed by said first exposing process.

[c10] The method in claim 8, wherein said second exposing process erases said first alignment mark by re-exposing an area of

said wafer where said first alignment mark was previously exposed.

[c11] The method in claim 8, further comprising repeating said second exposing process across said wafer, wherein each repetition of said second exposing process erases a previous alignment mark.

[c12] The method in claim 8, further comprising repeating said second exposing process across said wafer, wherein after said second exposing process is repeated across said wafer, alignment marks remain only on the edge of said wafer.

[c13] The method in claim 8, wherein said first exposing process and said second exposing process utilize the same mask.

[c14] The method in claim 13, wherein said mask includes a transparent region at a location where an image produced by said second exposing process overlaps said first alignment mark.

[c15] A method of repeatedly exposing a pattern across a wafer, said method comprising: repeatedly exposing said pattern across said wafer in a sequential stepping process, wherein said pattern includes at least one alignment mark, wherein each time said exposing process is repeated, the current exposure overlaps a portion of said wafer where said

pattern was previously exposed and thereby erases a previously exposed alignment mark by re-exposing an area of said wafer where said previously exposed alignment mark was located, and

wherein, after said exposing process is repeated across said wafer, alignment marks remain only on the edge of said wafer.

[c16] The method in claim 15, wherein said sequential stepping process utilizes the same mask to repeatedly expose said pattern at different locations across said wafer.

[c17] The method in claim 16, wherein said mask includes a transparent region at a location where an image produced by a subsequent exposing process overlaps a previously exposed alignment mark.

[c18] The method in claim 15, wherein, during said sequential stepping process, areas of exposure overlaps comprise one of kerf regions and support regions of said wafer positioned between semiconductor chips.

[c19] The method in claim 15, wherein after said sequential stepping process has stepped across said wafer, said process further comprises a second exposing process that exposes patterns in areas where alignment marks were erased.

[c20] The method in claim 15, wherein said sequential stepping process comprises one of a light-field exposure process and a

dark-field exposure process.